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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,616	06/29/2001	Roy Greeff	M4065.0411/P411	5708

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EXAMINER	
PHAN, RAYMOND NGAN	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,616	GREEFF ET AL.	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-127 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 112-127 is/are allowed.

6)☒ Claim(s) 1, 3-16, 36-45, 64-68, 75-76, 80-83, 86, 88-94, 96-98, 101-106, 110-111 is/are rejected.

7)☒ Claim(s) 2,17-35,46-63,69-74,77-79,84,85,87,95,99,100 and 107-109 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 1-127 are pending.

2. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2111.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-16, 36-45, 64-68, 75-76, 80-83, 86, 88-94, 96-98, 101-106, 110-111 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Werthein et al. (US No. 6,662,260) in view of Neal et al. (US No. 6,338,107).

In regard to claims 1, 36, 64-66, 75-76, 90, 93-94, 96-98, 101, 104-106, 110, Werthein et al. disclose a data transmission circuit, comprising: a first bus segment of a data bus (see col. 3, lines 34-57); a second bus segment of said data bus (see col. 3, lines 34-57); and a first switching circuit connected between said first and

second segments of said data bus, wherein said first switching circuit is configured to selectively connect said first and second segments of said data bus such that when said first switching circuit is in a first state, said first switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment (see col. 4, line 55 through col. 6, line 36). But Werthein et al. do not specifically disclose when said first switching circuit is in a second state, said second bus segment is disconnected from said first bus segment and data is passed through from said first bus segment to at least one I/O circuit and from said at least one I/O circuit to said first bus segment. However Neal et al. disclose the switching circuit is in a second state, said second bus segment is disconnected from said first bus segment and data is passed through from said first bus segment to at least one I/O circuit and from said at least one I/O circuit to said first bus segment (see col. 9, line 6 through col. 10, line 41). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Neal et al. within the system of Weithern et al. because it would provide an improved computer system having an expansion bus which allows the addition of peripheral devices to the system.

In regard to claim 3, Neal et al. disclose further comprising a plurality of switching circuits each configured to selectively pass data between segments of said data bus when in said first state, and between a segment of said data bus and at least one I/O circuit when in said second state (see col. 9, line 6 through col. 10, line 41). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Neal et al. within the system of Weithern et al. because it would provide an improved

computer system having an expansion bus which allows the addition of peripheral devices to the system.

In regard to claim 4, Neal et al. disclose wherein said first switching circuit includes a two-way switch that couples said first and second bus segments when said switching circuit is in said first state, and couples said first bus segment to said at least one I/O circuit when said switching circuit is in said second state (see col. 9, line 6 through col. 10, line 41). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Neal et al. within the system of Wertheim et al. because it would provide an improved computer system having an expansion bus which allows the addition of peripheral devices to the system.

In regard to claims 5, 37, 41, 83, 86, Wertheim et al. disclose wherein said first switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on a command and address bus (see col. 5, line 15 through col. 6, line 53).

In regard to claims 6, 38, 42, 111, Wertheim et al. disclose wherein said first switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on said data bus (see col. 5, line 15 through col. 6, line 53).

In regard to claims 7, 43, Neal et al. disclose wherein said first switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on at least one dedicated selection data path (see col. 9, line 6 through col. 10, line 41). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Neal et al. within the system of Weithern

et al. because it would provide an improved computer system having an expansion bus which allows the addition of peripheral devices to the system.

In regard to claims 8, 44, 88, Wertheim et al. disclose wherein said data bus is a multidrop bus (see col. 3, lines 9-58).

In regard to claims 9, 45, 89, Wertheim et al. disclose wherein said data bus is a substantially stubless data bus (see col. 3, lines 9-53).

In regard to claims 10, 39, 67, 91, 102, Wertheim disclose wherein said first switching circuit includes a p-channel field-effect transistor (FET) switch (see col. 6, line 53 through col. 7, line 52).

In regard to claims 11, 40, 68, 92, 103, Wertheim et al. disclose wherein said first switching circuit includes a p-channel field-effect transistor (FET) switch and an n-channel FET switch (see col. 6, line 53 through col. 7, line 52).

In regard to claim 12, even though the teachings of Wertheim et al. or Neal et al. do not specifically disclose wherein said first switching circuit is formed using Gallium Arsenide (GaAs) semiconductor technology, however one skilled in the art would have understood that they can choose to fabricate on the surface of a semiconductor wafer of silicon, gallium arsenide, or indium phosphide to fulfill their need.

In regard to claim 13, Wertheim et al. disclose wherein said first switching circuit has a programmable drive strength (see col. 5, lines 15-52).

In regard to claim 14, Wertheim et al. disclose wherein said first switching circuit is located on a motherboard (see col. 3, lines 9-58).

In regard to claim 15, Wertheim et al. disclose wherein said first switching circuit is located on a memory module (see col. 3, lines 9-58).

In regard to claim 16, Wertheim et al. disclose wherein said first switching circuit is located on a same integrated circuit chip as a memory device (see col. 3, lines 9-58).

In regard to claim 80, Wertheim et al. disclose wherein said first data bus transmits analog signals (see col. 3, lines 9-58).

In regard toc claim 81, Wertheim et al. disclose wherein said first data bus transmits digital signals (see col. 3, lines 9-58).

In regard to claim 82, even though the teachings of Wertheim et al. or Neal et al. do not specifically disclose wherein said first data bus transmits radio-frequency (RF) signals, however one skilled in the art would have understood that they can choose to have suitable of signals to fulfill their need.

Allowable Subject Matter

6. Claims 112-127 are allowable over the prior of records.

7. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claim 112 is allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts which teach a method of data communication between devices in an electronic circuit, comprising: connecting an interface circuit having first and second sets of I/O pins to respective first and second segments of a first data bus that operates at a first data rate; connecting said interface circuit to a second data bus that operates at a second data rate; receiving and transmitting data on said first data bus using said first and second sets of I/O pins; receiving and transmitting data on said second

data bus; selectively converting data received from one of said first and second data buses for use on the other of said first and second data buses.

8. Claims 2, 17-35, 46-63, 69-74, 77-79, 84-85, 87, 95, 99-100, 107-109 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 2, 17-18, 46-47, 69, 71-74, 77-79, 84-85, 87, 95, 99-100, 107-109 are allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts which teach a second switching circuit connected between said second segment of said data bus and a third segment of said data bus, wherein said second switching circuit is configured to selectively connect said second and third segments of said data bus such that when said second switching circuit is in a first state, said second switching circuit passes data through from said second bus segment to said third bus segment and from said third bus segment to said second bus segment, and when said second switching circuit is in a second state, said third bus segment is disconnected from said second bus segment and data is passed through from said second bus segment to at least one I/O circuit and from said at least one I/O circuit to said second bus segment (claim 2); wherein said first switching circuit receives a command selecting at least one attached I/O circuit for point-to-point communications, selects said second state of said first switching circuit to disconnect said first bus segment from said second bus segment, and passes data between said first bus segment and said at least one attached selected I/O circuit (claims 17, 46); wherein said data bus is a

first data bus having a first number of data paths, and said first switching circuit is further configured to connect to a second data bus having a second number of data paths, wherein said first switching circuit is connected between said first and second data buses for selectively receiving data on said first data bus and placing said data on said second data bus and selectively receiving data on said second data bus and placing said data on said first data bus (claims 18, 47); wherein said interface circuit further comprises at least one conversion circuit which performs a data rate conversion between said first and second data buses (claim 69); wherein said interface circuit further comprises a multiplexer and a demultiplexer which perform data rate conversions for data received on said first data bus that is placed on said second data bus and for data received on said second data bus that is placed on said first data bus (claim 71); wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses (claim 72); wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses (claim 73); wherein said first number of data paths is less than said second number of data paths (claim 74); wherein said interface circuit is connected to said first bus segment of said first data bus via a first set of I/O pins and to said second bus segment via a second set of I/O pins, and I/O pins of said first set are connected to respective I/O pins of said second set through said switching circuit (claim 77); wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates (claim 78); wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates (claim 79); wherein said selection signal controls said switching circuit, whereby said first

segment is disconnected from said second segment while data is being received from said first data bus (claims 84, 87); wherein said interface circuit is further configured to selectively receive data on said second data bus and place said data on said first data bus (claim 85); wherein said plurality of system devices includes a bus terminator (claim 95); wherein a switchable terminator is included in at least one of said plurality of system devices (claim 99); wherein a programmable terminator is included in at least one of said plurality of system devices (claim 100); wherein said selective passing of data includes configuring said at least one switching circuit to pass data during WRITE operations (claim 107); wherein said selective passing of data includes configuring said at least one switching circuit to pass data between a memory controller and a selected I/O device during READ operations (claim 108); wherein said selective passing of data includes configuring said at least one switching circuit to pass data between a memory controller and a selected I/O device during WRITE operations (claim 109).

The remaining claims, not specifically mentioned, are allowed for the same rationale from the parent claim by dependency.

Conclusion

10. Claims 1, 3-16, 36-45, 64-68, 75-76, 80-83, 86, 88-94, 96-98, 101-106, 110-111 are rejected. Claims 2, 17-35, 46-63, 69-74, 77-79, 84-85, 87, 95, 99-100, 107-109 are objected. Claims 112-127 are allowed.

11. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Gerhold (US No. 4,470,114) discloses a high speed interconnection network for a cluster of processors.

Foo (US No. 6,662,256) discloses a sequential bus architecture.

Kelley et al. (US No. 6,182,178) disclose a method and system for supporting peripheral component interconnect (PCI) peer-to-peer access across a PCI host bridge supporting multiple PCI buses.

Bruce et al. (US No. 5,978,880) disclose a multi-segmented bus and method of operation.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**raymond.phan@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Raymond Phan
5/15/04